UNIVERSITY OF KERALA

B. TECH. DEGREE COURSE

(2013 SCHEME)

SYLLABUS FOR

IV SEMESTER

ELECTRONICS and COMMUNICATION ENGINEERING

SCHEME -2013

IV SEMESTER

ELECTRONICS and COMMUNICATION ENGINEERING (T)

Course No	Name of subject	Credits	Weekly load, hours			C A Marks	Exam Duration Hrs	U E Max Marks	Total Marks
			L	T	D/ P				
13.401	Engineering Mathematics III - Probability & Random Processes (AT)	4	3	1	-	50	3	100	150
13.402	Humanities (ACHPT)	3	3	-	-	50	3	100	150
13.403	Computer Organisation & Architecture (AT)	3	2	1	-	50	3	100	150
13.404	Digital Signal Processing (AT)	4	3	1	-	50	3	100	150
13.405	Computer Programming (T)	4	2	-	2	50	3	100	150
13.406	Analog Integrated Circuits (T)	3	2	1		50	3	100	150
13.407	Digital Integrated Circuits Lab (T)	4	-	-	4	50	3	100	150
13.408	Analog Integrated Circuits Lab (T)	4	-	-	4	50	3	100	150
	Total	**29**	**15**	**4**	**10**	**400**		**800**	**1200**

13.401 ENGINEERING MATHEMATICS -III (AT)
(PROBABILITY & RANDOM PROCESSES)

Teaching Scheme: 3(L) - 1(T) - 0(P) **Credits**: 4

Course Objective:

- *To provide a basic understanding of random variables and probability distributions.*
- *To give a basic idea about Random process - its classification, types and properties and their applications in engineering fields.*

Module – I

Random Variables -Discrete and continuous random variables -Probability distributions.- Mathematical Expectations and properties

Special probability distributions-Binomial distribution, Poisson distribution, Poisson approximation to Binomial, Uniform distribution, Exponential Distribution, Normal distribution- mean and variance of the above distributions-Distribution fitting (Binomial, Poisson)

Module – II

Multiple random variables -Joint and marginal distributions-Expectation involving two or more random variables- independence, correlation and covariance of pairs of random variables, central limit theorem (no proof).

Random processes-Types of random processes-Ensemble mean-Wide sense stationary (WSS) process. - Autocorrelation, autocovariance and their properties.

Module – III

Power spectral density (PSD)-PSD of real processes and its properties. Relation between autocorrelation and power spectral density. Transmission of Random process through a linear Filter

Ergodicity-Time averages of sample functions, ergodic processes, mean ergodic theorem (without proof).

Discrete time Markov chain -Transition probability matrix, Chapman Kolmogorov theorem (without proof), computation of probability distribution, steady state probabilities.

Module – IV

Poisson process-mean and variance, properties, probability distribution of inter arrival times. Random telegraph process, Gaussian process – properties.

Basic Queueing theory- Queueing systems, Little's formula (no proof), M/M/1 queues with finite/infinite capacity and M/M/c queues with infinite capacity-computation of steady state probabilities, mean number of customers, mean waiting times etc.

References:

1. Garcia A. L., *Probability and Random Processes for Electrical Engineering*, 2/e, Pearson Education, 2007.
2. Ibe O. C., *Fundamentals of Applied Probability and Random Processes*, Academic Press, 2005.
3. Gubner J. A., *Probability and Random Processes for Electrical and Computer Engineers*, Cambridge University Press, 2006.
4. Sundarapandian V., *Probability Statistics and Queueing Theory*, 2/e, Prentice Hall, 2009.

Internal Continuous Assessment *(Maximum Marks-50)*

50% - Tests (minimum 2)

30% - Assignments (minimum 2) such as home work, problem solving, quiz, literature survey, seminar, term-project, software exercises, etc.

20% - Regularity in the class

University Examination Pattern:

Examination duration: 3 hours *Maximum Total Marks: 100*

The question paper shall consist of 2 parts.

Part A (20 marks) - Five Short answer questions of 4 marks each. All questions are compulsory. There should be at least one question from each module and not more than two questions from any module.

Part B (80 Marks) - Candidates have to answer one full question out of the two from each module. Each question carries 20 marks.

Course Outcome:

After successful completion of this course, the students will be able to master the concepts of probability and Random analysis which they can use later in their career to solve problems related to engineering fields.

13.402 HUMANITIES (ACHPT)

Teaching Scheme: 3(L) - 0(T) - 0(P) **Credits**: 3

Course Objectives:

- *To explore the way in which economic forces operate in the Indian Economy.*
- *The subject will cover analysis of sectors, dimensions of growth, investment, inflation and the role of government will also be examined.*
- *The principle aim of this subject is to provide students with some basic techniques of economic analysis to understand the economic processes with particular reference to India.*
- *To give basic concepts of book keeping and accounting*

PART I ECONOMICS (2 periods per week)

Module – I

Definition of Economics –Central Economic Problems – Choice of techniques –Production possibility curve – Opportunity Cost-Micro & Macro Economics

Meaning of Demand – Utility-Marginal Utility and Law of Diminishing Marginal Utility-Law of demand - Determinants of Demand – Changes in Demand – Market Demand—Demand, forecasting-Meaning of supply-Law of Supply- Changes in Supply-- Market Price Determination – Implications of Government Price Fixation

Production function – Law of Variable proportion – Returns to scale – Iso-quants and Isocost line- Least cost combination of inputs – Cost concepts – Private cost and Social Cost -

Short run and Long run cost- cost curves – Revenue – Marginal, Average and Total Revenue-Break even Analysis

Module – II

National Income concepts - GNP – GDP – NNP– Per Capita Income – Measurement of National Income-Output method- Income method and Expenditure method -Sectoral Contribution to GDP– Money-Static and Dynamic Functions of Money-Inflation – causes of inflation – measures to control inflation – Demand Pull inflation – cost push inflation – Effects of Inflation – Deflation.

Global Economic Crisis India's Economic crisis in 1991 – New economic policy – Liberalization – Privatization and Globalization-Multinational Corporations and their impacts on the Indian Economy- Foreign Direct Investment (FDI) Performance of India-Issues and Concerns. Industrial sector in India – Role of Industrialization -Industrial Policy Resolutions-Industry wise analysis – Electronics – Chemical – Automobile – Information Technology.

Environment and Development – Basic Issues – Sustainable Development- Environmental Accounting – Growth versus Environment – The Global Environmental Issues- Poverty- Magnitude of Poverty in India- -Poverty and Environment

PART-II- ACCOUNTANCY (1 Period per week)

Module – III

Book-Keeping and Accountancy- Elements of Double Entry- Book –Keeping-rules for journalizing-Ledger accounts-Cash book- Banking transactions- Trial Balance- Method of Balancing accounts-the journal proper(simple problems).

Final accounts: Preparation of trading and profit and loss Account- Balance sheet (with simple problems) - Introduction to accounting packages (Description only).

References

1. Dewett K. K., *Modern Economic Theory,* S Chand and Co. Ltd., New Delhi, 2002.
2. Todaro M., *Economic Development*, Addison Wesley Longman Ltd., 1994.
3. Sharma M. K., *Business Environment in India,* Commonwealth Publishers, 2011.
4. Mithani D. M., *Money, Banking, International Trade and Public Finance*, Himalaya Publishing House, New Delhi, 2012.
5. Dutt R. and K. P. M. Sundaran*, Indian Economy,* S. Chand and Co. Ltd., New Delhi, 2002.
6. Varian H. R., *Intermediate Micro Economics,* W W Norton & Co. Inc., 2011.
7. Koutsoyiannis A., *Modern Micro-economics,* MacMillan, 2003.
8. Batliboi J. R., *Double Entry Book-Keeping,* Standard Accountancy Publ. Ltd., Bombay, 1989.
9. Chandrasekharan Nair K. G., *A Systematic approach to Accounting*, Chand Books, Trivandrum, 2010.

Internal Continuous Assessment *(Maximum Marks-50)*

50% - Tests (minimum 2)

30% - Assignments (minimum 2) such as home work, problem solving, literature survey, seminar, term-project, software exercises, etc.

20% - Regularity in the class

University Examination Pattern:

Examination duration: 3 hours *Maximum Total Marks: 100*

The question paper shall consist of 2 parts. Part I and Part II to be answered in separate answer books.

Part I Economics *(70 marks) – Part I shall consist of 2 parts.*

Part A (20 Marks) - Ten short answer questions of 2 marks each, covering entire syllabus of Part I (five questions each from Module I and Module II). All questions are compulsory.

Part B (50 marks) - Candidates have to answer one full question out of the two from Part I (Module I and Module II). Each question carries 25 marks.

Part II Accountancy *(30 marks)*

Candidates have to answer two full questions out of the three from Part II (Module III). Each question carries 15 marks.

Course outcome:

- *The students will be acquainted with its basic concepts, terminology, principles and assumptions of Economics.*
- *It will help students for optimum or best use of resources of the country.*
- *It helps students to use the understanding of Economics of daily life.*
- *The students will get acquainted with the basics of book keeping and accounting.*

13.403 COMPUTER ORGANISATION & ARCHITECTURE (AT)

Teaching Scheme: 2(L) - 1(T) - 0(P) **Credits**: 3

Course Objectives:

- *To have a thorough understanding of the basic structure and operation of a digital Computer and to analyse their performance*
- *To discuss in detail the operation of the arithmetic unit including the algorithms &implementation of fixed-point and floating-point addition, subtraction, multiplication &division.*
- *To study the different ways of communicating with I/O devices and standard I/O interfaces.*
- *To study the issues affecting modern processors including cache and virtual Memories, pipeline etc.*

Module – I

Functional units of a Computer - Von Neuman Architecture, Harvard Architecture - CISC and RISC.

Computer Arithmetic - Implementing addition, subtraction, multiplication and division - Floating point representation - Floating point operations & their implementation.

MIPS – architecture, addressing modes, instruction format and instruction set. Translating a C program into MIPS assembly language and machine codes.

Module – II

Design of Data path and Control (based on MIPS instruction set) - Design of data path for memory reference, arithmetic/logical (add, sub, and, or) and branch instructions. Control of the single clock cycle implementation and Multi cycle implementation - Fetch, Decode, Execute and Memory access cycles. Design of control unit - Hardwired and Micro programmed control.

Module – III

Memory hierarchy - Main Memory, Cache Memory - Elements of Cache design, mapping techniques - Replacement algorithm - Cache performance - interleaved memory, Virtual memory - Page Table, Page Replacement, Address translation. Internal Memory technology - Semiconductor main memory, DRAM and SRAM, Types of ROM. External Memory - Magnetic Disk, RAID, Optical Memory.

Module – IV

Enhancing Performance – Pipelining, overview of pipelining, pipelined data path, pipelined control, data hazards and forwarding, data stalls, control hazards, branch hazards.

Peripheral devices, I/O interface, Modes of Transfer, Priority Interrupt, Direct Memory Access, Input-Output Processor and Serial Communication. I/O Controllers, Asynchronous data transfer, Strobe Control, Handshaking.

References:

1. Patterson D. A. and J. L. Hennessy, *Computer Organisation and Design – The Hardware / Software Interface*, 3/e, Elsevier, 2013.
2. Stalling W., *Computer Organization & Architecture*, 9/e, Pearson Education, 2013.
3. Hayes J. P., *Computer Architecture and Organisation*, 3/e, McGraw Hill, 1998.
4. Patterson D. A. and J. L. Hennessy, *Computer Architecture – A Quantitative Approach,* 4/e, Elsevier, 2006.
5. Hamacher C., Z. Vranesic and S. Zaky, *Computer Organisation*, 5/e, Tata McGraw Hill, 2013.

Internal Continuous Assessment *(Maximum Marks-50)*

50% - Tests (minimum 2)

30% - Assignments (minimum 2) such as home work, problem solving, quiz, literature survey, seminar, term-project, software exercises, etc.

20% - Regularity in the class

University Examination Pattern:

Examination duration: 3 hours *Maximum Total Marks: 100*

The question paper shall consist of 2 parts.

Part A (20 marks) - Ten Short answer questions of 2 marks each. All questions are compulsory. There should be at least two questions from each module and not more than three questions from any module.

Part B (80 Marks) - Candidates have to answer one full question out of the two from each module. Each question carries 20 marks.

***Note:** Question paper should contain minimum 40% and maximum 60% Problems, Design and Analysis.*

Course Outcome:

After the completion of this course, students will get necessary foundation regarding the computer architecture and its peripherals.

13.404 DIGITAL SIGNAL PROCESSING (AT)

Teaching Scheme: 3(L) - 1(T) - 0(P) **Credits**: 4

Course Objective:

- *Introduction to the principle, algorithms and applications of modern Digital Signal Processing.*
- *To give an understanding of essential DSP principles and Applications and to demonstrate the importance of the subject to electronics engineering as practised today.*

Module – I

The Discrete Fourier Transform , Properties of DFT, Linear Convolution and correlation Methods based on the DFT, Frequency Analysis of Signals using DFT. Computation of DFT: Decimation in time and decimation in frequency FFT Algorithms (Radix 2 only), Efficient computation of DFT of Two Real Sequences and a 2N-Point Real Sequence, IDFT computation using DFT. Introduction to DCT and properties.

Module – II

Design of FIR Filters- Symmetric and Antisymmetric FIR Filters, Design of linear phase FIR Filters using Window method and Frequency Sampling Method, Design of Optimum Equiripple Linear-Phase FIR Filters. Design of IIR Digital Filters from Analog Filters (Butterworth and Chebyshev)- IIR Filter Design by Impulse Invariance, IIR Filter Design by Bilinear Transformation, Frequency Transformations in the Analog and Digital Domain.

Module – III

Filter structures: FIR Systems- Direct Form, Cascade Form and Lattice Structure. IIR Systems- Direct Form, Transposed Form, Cascade Form and Parallel Form. Lattice structures for FIR and IIR filters. Analysis of finite word length effects- Quantization noise, round off errors, input and output quantization error, limit cycles in IIR filters, round off errors in FFT algorithms.

Module – IV

Multi-rate Digital Signal Processing- Decimation and Interpolation (Time domain and Frequency Domain Interpretation), Sampling Rate Conversion, Multistage Implementation of Sampling-Rate Conversion, Applications of Multi-rate Signal Processing- Sub band Coding, Trans-multiplexers.

Computer architecture for signal processing - Architecture of TMS320C6713 processor.

Programming Tools for DSP Processors.

References:

1. Oppenheim A. V., R. W. Schafer and J. R. Buck*, Discrete Time Signal Processing*, 2/e, Prentice Hall, 2007.
2. Proakis J. G. and D. G. Manolakis, *Digital Signal Processing*, 4/e, Prentice Hall, 2007.
3. Chassaing R. and D. Reay *Digital Signal Processing and Applications with the TMS320C6713 and TMS320C6416 DSK, John Wiley &Sons,* 2011.
4. Mitra S. K., *Digital Signal Processing: A Computer Based Approach*, 4/e McGraw Hill, 2011.
5. Ifeachor E. and B. W. Jervis, *Digital Signal Processing*, 2/e, Pearson Education, 2009.
6. Vaidyanathan P. P., *Multirate Systems and Filter Banks*, Pearson Education, 2008.
7. Baese U. M., *Digital Signal Processing with FPGAs*, 3/e, Springer, 2007.
8. Ingle V. K. and J. G. Proakis, *Digital Signal Processing A MATLAB based Approach,* 3/e, Cengage, 2008.
9. Kumar A. A., *Digital Signal Processing*, Prentice Hall, 2012.

Internal Continuous Assessment *(Maximum Marks-50)*

50% - Tests (minimum 2)

30% - Assignments (minimum 2) such as home work, problem solving, quiz, literature survey, seminar, term-project, software exercises, etc.

20% - Regularity in the class

University Examination Pattern:

Examination duration: 3 hours *Maximum Total Marks: 100*

The question paper shall consist of 2 parts.

Part A (20 marks) - Ten Short answer questions of 2 marks each. All questions are compulsory. There should be at least two questions from each module and not more than three questions from any module.

Part B (80 Marks) - Candidates have to answer one full question out of the two from each module. Each question carries 20 marks.

***Note:** Question paper should contain minimum 60% and maximum 80% Problems, Derivations and Proofs.*

Course Outcome:

After the course student will understand the principle of digital signal processing and applications. The utilization of DSP to electronic engineering will also studied.

13.405 COMPUTER PROGRAMMING (T)

Teaching Scheme: 2(L) - 0(T) - 2(P) **Credits:** 4

Course Objectives:

- *To provide strong foundation in programming and in C++*

Module – I

Basic stricture of a C++ program - Data types and Operators – Enumerated data types – Type conversion – Conditional statements and loops – Arrays (one and two dimensional) and strings – Functions - Recursive functions – Storage class specifiers.

Module – II

Pointers – Pointer to arrays and strings – Pointer to pointer – Array of pointers – Structures and Unions - new and delete operators for dynamic memory management

Classes and objects – private, public and protected variables - Constructors and Destructors – Array of class objects – Pointer and classes – 'this' pointer - Inline member Functions – Static Class Members.

Module – III

Function overloading, Operator overloading - Friend functions - Inheritance - Polymorphism - Virtual functions.

Data File Operations - Exception handling – Creating and Manipulating String Objects.

Module – IV

Data Structures: Linked lists (single) - basic operations - Stack and Queues - basic operations using arrays and linked lists.

Searching and Sorting – Linear Search and Binary Search - Bubble sort – Insertion sort – Selection sort.

References:

1. Stroustrup B., *The C++ Programming Language*, 4/e, Addison-Wesley, 2013.
2. Balagurusamy E., *Object Oriented Programming with C++*, 6/e, Tata McGraw Hill, 2013.
3. Aho A. V., J. E. Hopcroft and J. D. Ullman, *Data Structures and Algorithms*, Pearson, 2005.
4. Ravichandran D., *Programming with C++*, 3/e, Tata McGraw Hill, 2011.
5. Kanetkar Y., *Let us C++,* BPB Publications, 2003.
6. Eckel B., *Thinking in C++*, *Vol.* I, 2/e, Prentice Hall, 2000.

7. Eckel B. and C. Allison, *Thinking in C++*, *Vol.* II, Prentice Hall, 2004.
8. Samanta D., *Classic Data Structures*, Prentice Hall, 2006.
9. Sagar A. D., *Expert Data Structures using C/C++,* BPB Publications, 2009.
10. Kanetkar Y., *Data Structures through C++,* BPB Publications, 2003.

Internal Continuous Assessment *(Maximum Marks-50)*

50% - Tests (minimum 2)

30% - Assignments (minimum 2) such as home work, problem solving, quiz, literature survey, seminar, term-project, software exercises, etc.

20% - Regularity in the class

University Examination Pattern:

Examination duration: 3 hours *Maximum Total Marks: 100*

The question paper shall consist of 2 parts.

Part A (20 marks) - Ten Short answer questions of 2 marks each. All questions are compulsory. There should be at least two questions from each module and not more than three questions from any module.

Part B (80 Marks) - Candidates have to answer one full question out of the two from each module. Each question carries 20 marks.

Note: *Question paper should contain minimum 60% and maximum 80% Programming and Algorithms.*

Course Outcome:

After successful completion of the course, the students will have the confidence and knowledge to write useful, complex and multifunction programs.

13.406 ANALOG INTEGRATED CIRCUITS (T)

Teaching Scheme: 2(L) - 1(T) - 0(P) **Credits**: 3

Course Objective:

- *To equips the students with a sound understanding of fundamental concepts of operational amplifiers.*
- *To know the diversity of operations that the op amp can perform in a wide range of applications.*
- *To study the different types of ICs and its applications.*

Module – I

Operational Amplifier: Introduction, Ideal op-amp parameters, Non ideal op-amp. Effect of finite open loop gain, bandwidth and slew rate on circuit performance. Inverting and non-inverting amplifier, summing amplifier, integrator, differentiator. Differential amplifiers, Instrumentation amplifiers, V to I and I to V converters, Comparators, precision rectifiers, Log and antilog amplifier.

Module – II

Oscillators -Phase-shift, Wein-Bridge, Multivibrators - Astable, Monostable, Schmitt Trigger, Square and triangular waveform generator.
Filters: Butterworth 1^{st} order Low pass and high pass. Biquadratic filter (single op-amp with finite gain non inverting-Sallen and key) of Low pass, High pass, Band pass and Notch filters. Generalized Impedance Converter and its applications.

Module – III

Switched capacitor Resistor, switched capacitor Integrator, First order SC filter.
D/A converters: DAC characteristics and Parameters- Weighted resistor, R-2R network, DAC080.
A/D converter: ADC characteristics, Types - Dual slope, Counter ramp, Successive approximation, flash ADC - AD670. Principle of oversampled ADC.

Module – IV

Analog multipliers – emitter coupled pair as simple multiplier, Gilbert multiplier cell, four quadrant multiplier, Gilbert multiplier as a balanced modulator and phase detector, AD532.

Basic PLL topology and principle, Major building blocks of PLL – analog and digital phase detector, VCO, filter. Applications of PLL. Monolithic PLL 565.

Monolithic Voltage Regulators – three terminal voltage regulators 78XX and 79XX series, IC723 and its Applications, Current boosting, short circuit and fold back protection.

References:-

1. Salivahanan S. and V. S. K. Bhaaskaran, *Linear Integrated Circuits*, Tata McGraw Hill, 2008.
2. Razavi B., *Designs Of Analog CMOS Integrated Circuits*, Tata McGraw Hill, 2008.
3. Franco S., *Design with Operational Amplifiers and Analog Integrated Circuits*, 3/e, Tata McGraw Hill, 2008.
4. Gayakwad R. A., *Op-Amps and Linear Integrated Circuits*, Prentice Hall, 4/e, 2010.
5. Soclof S., *Design & Applications of Analog Integrated Circuits*. PHI, 2008
6. Johns D. A. and K. Martin, *Analog Integrated Circuit Design*, Wiley India, 2008.
7. Roy D. C. and S. B. Jain, *Linear Integrated Circuits*, New Age International, 3/e, 2010.
8. Nair B. S., *Linear Integrated Circuits*, Wiley India, 2009.
9. Botkar K. R., *Integrated Circuits*, 10/e, Khanna Publishers, 2010.
10. Coughlin R. F. and F. F. Driscoll, *Operational Amplifiers and Linear ICs*, 6/e, Prentice Hall, 2012.

Internal Continuous Assessment *(Maximum Marks-50)*

50% - Tests (minimum 2)

30% - Assignments (minimum 2) such as home work, problem solving, quiz, literature survey, seminar, term-project, software exercises, etc.

20% - Regularity in the class

University Examination Pattern:

Examination duration: 3 hours *Maximum Total Marks: 100*

The question paper shall consist of 2 parts.

Part A (20 marks) - Ten Short answer questions of 2 marks each. All questions are compulsory. There should be at least two questions from each module and not more than three questions from any module.

Part B (80 Marks) - Candidates have to answer one full question out of the two from each module. Each question carries 20 marks.

***Note:** Question paper should contain minimum 50% and maximum 70% Design, Analysis and Problems.*

Course Outcome:

At the end of the course, students shall be able to design electronic circuits using ICs.

13.407 DIGITAL INTEGRATED CIRCUITS LAB (T)

Teaching Scheme: 0(L) - 0(T) - 4(P) **Credits**: 4

Course Objective :

- *To familarise various types of Digital ICs.*
- *To assemble digital circuits using ICs and study the performance.*

List of Experiments:

1. Realization of functions using basic and universal gates.
2. Half adder, Full adder using NAND and NOR only.
3. Half subtractor, full subtractor using NAND and NOR only..
4. 4 bit adder/subtractor and BCD adder using 7483.
5. Binary to Gray and Gray to Binary converters.
6. 2/3 bit binary comparator.
7. BCD to Decimal and BCD to 7 segment decoder & display
8. Multiplexers, De-multiplexers using gates and ICs. (74150, 74154)
9. Realization of combinational circuits using MUX & DEMUX.
10. Astable & Monostable multivibrators using 74121 & 555.
11. Realization of RS, T, D, JK and Master Slave flip-flops using gates.
12. Synchronous counters using flip flops.
13. Asynchronous counters using flip flops.
14. Realization of counters using IC's (7490, 7492, 7493).
15. Random sequence generator.
16. Shift Registers, Ring counter and Johnson counter (using flip flops and 7495)
17. Implementation of digital clock, digital timer, event counter, token display –as class project.
18. Simulation using VHDL –simple arithmetic circuits, flip flops and counters.

Internal Continuous Assessment *(Maximum Marks-50)*

40% - Test
40% - Class work and Record
20% - Regularity in the class

University Examination Pattern:

Examination duration: 3 hours *Maximum Total Marks: 100*

Questions based on 1 to 16 experiments prescribed in the list.

25% - Circuit Design

15% - Performance (Wiring, use of equipment/instruments and trouble shooting)

35% - Result

25% - Viva voce

Candidate shall submit the certified fair record for endorsement by the external examiner.

Course Outcome:

From the practical exposure, the students can design digital circuits such as registers, counters, arithmetical circuits, flip flops etc.

13.408 ANALOG INTEGRATED CIRCUITS LAB (T)

Teaching Scheme: 0(L) - 0(T) - 4(P) **Credits**: 4

Course Objective :

- *To enable the students to have the practical knowledge of different analog ICs.*
- *To study the specifications of ICs and to design circuits using ICs.*

List of Experiments:

1. Familiarization of Operational amplifiers - Inverting and Non inverting amplifiers, frequency response, Adder, Integrator, comparators.
2. Measurement of Op-Amp parameters.
3. Difference Amplifier and Instrumentation amplifier.
4. Schmitt trigger circuit using Op –Amps.
5. Astable and Monostable multivibrator using Op -Amps.
6. Triangular and square wave generators using Op- Amplifier.
7. Wien bridge oscillator using op-amplifier- without & with amplitude stabilization
8. RC Phase shift Oscillator.
9. Precision rectifiers using Op-Amp.
10. Active second order filters using Op-Amp. (LPF, HPF, BPF and BSF)
11. Filters using gyrator circuits.
12. Window Comparator using LM311.
13. IC voltage regulators (723), low & high voltage regulation Short circuit and Fold back protection.
14. A/D converters- counter ramp and flash type.
15. D/A Converters- ladder circuit.

Internal Continuous Assessment *(Maximum Marks-50)*

40% - Test
40% - Class work and Record
20% - Regularity in the class

University Examination Pattern:

Examination duration: 3 hours *Maximum Total Marks: 100*

Questions based on the list of experiments prescribed

25% - Circuit Design

15% - Performance (Wiring, use of equipment/instruments and trouble shooting)

35% - Result

25% - Viva voce

Candidate shall submit the certified fair record for endorsement by the external examiner.

Course Outcome:

After completion the course student will understand the working of circuits using ICs and will be able to design circuits using ICs